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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Tyler A. Lowrey Et Al.

§ Group Art Unit: 2827

Serial No.: 10/633,872

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Filed: August 4, 2003

For: Read Bias Scheme For Phase  
Change Memories

§ Examiner: T. Le

§ Atty. Dkt. No.: ITO.0046US  
(P16201)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicant submits the references listed on the attached form PTO 1449, copies of which are enclosed. A copy of a communication dated April 15, 2005 from a foreign patent office in a counterpart application is also enclosed. I, the undersigned, hereby certify that each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Information Disclosure Statement. Please apply any charges or credits to Deposit Account No. 20-1504 (ITO.0046US).

Respectfully submitted,

May 12, 2005

Date

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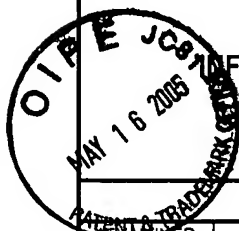
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Monica Jacobs

**INFORMATION DISCLOSURE CITATION**

(Use several sheets if necessary)

ATTY DOCKET NO.

ITO.0046US (P16201)

SERIAL NO.

10/633,872

APPLICANT(S):

Tyler A. Lowrey et al.

FILING DATE:

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GROUP ART UNIT:

2827

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A.	4,199,692	04/22/1980	Neale			
	B.	5,536,947	07/16/1996	Klersy et al.			
	C.						
	D.						

**U.S. PATENT APPLICATION PUBLICATIONS**

	E.	US 2004/0228159	11/18/2004	Kostylev et al.			
	F.						
	G.						
	H.						

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	I.	EP 1 489 623	12/22/2004	Europe				
	J.	WO 00/57498	09/28/2000	PCT				
	K.	WO 2004/055828	07/01/2004	PCT				
	L.	WO 2004/055899	07/01/2004	PCT				
	M.	WO 2005/017904	02/24/2005	PCT				

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

	N.	Yi-Chou Chen et al., <i>An Access-Transistor-Free (0T/1R) Non-Volatile Resistance Random Access Memory (RRAM) Using A Novel Threshold Switching, Self-Rectifying Chalcogenide Device</i> , Intl. Electron Devices Mtg. 2003, IEDM, Technical Digest, Washington, DC Dec. 8-10, 2003, New York, NY: IEEE, pgs. 905-908.						
	O.	Agostino Pirovano et al., <i>Low-Field Amorphous State Resistance And Threshold Voltage Drift In Chalcogenide Materials</i> , IEEE Transactions On Electron Devices, IEEE Inc., New York, NY, Vol. 51, No. 5, May 2004, pgs. 714-719.						
	P.	F. Pellizzer et al., <i>Novel <math>\mu</math>Trench Phase-Change Memory Cell For Embedded And Stand-Alone Non-Volatile Memory Applications</i> , VLSI Technology, 2004, Digest of Technical Papers 2004 Symposium, Honolulu, HI, June 15-17, 2004, Piscataway, NJ, IEEE, June 15, 2004, pgs. 18-19.						
	Q.							
	R.							

EXAMINER

DATE CONSIDERED

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.